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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/625,178 | 07/25/2000 | Hiroki Nakamura | F98ED0762 | 7254 |

7590 12/28/2001

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| EXAMINER |
|---|
| MAI, ANH D |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2814 | |

DATE MAILED: 12/28/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/625,178 | NAKAMURA, HIROKI | |
| | Examiner | Art Unit | |
| | Anh D. Mai | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *21-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of Group I, claims 1-20, in Paper No. 6 is acknowledged.

### *Specification*

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Drawings*

3. Figure 8A-C should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

4. Claim 5 is objected to because of the following informalities:

Lines 3-4, "the second dummy layer" should be --the second dummy pattern-- .

Line 7, "dummy layer" should be --dummy pattern--.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5-10 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "whereby, the first dummy pattern is formed the fourth insulating layer which is formed on the first dummy *layer* (should be pattern), and the circuit patterns are formed on the fourth insulating layer" in lines 6-8. There is insufficient antecedent basis for this limitation in the claim.

A pattern can not be formed on itself. It appears that the fourth insulating layer 302 is formed on the second dummy pattern 300a (Fig. 3A) rather than on the first dummy pattern 304a.

Claim 13 recites the limitation "the second dummy pattern" in line 2. There is insufficient antecedent basis for this limitation in the claim.

The "second dummy pattern" should be --third dummy pattern--, since there is no second dummy pattern in either claim 1 nor claim 11.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-6 and 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha et al. (JP-10-270445) in view of Hosoda et al. (JP-08-181208).

Yamaha teaches a semiconductor device substantially similar as claimed including:

a semiconductor substrate (10) having a grid-line area and a chip area, the chip area having a circuit area (RA) and a dummy area (RB);

circuit patterns (12s) formed on the substrate in the circuit area;

a first dummy pattern (13) which is formed of the same material as the circuit pattern, formed in the dummy area (RB), the dummy pattern encompassing the circuit area;

a first insulating layer (14a) formed on an entire surface of the semiconductor substrate;

a second insulating layer (14b) formed only on the first insulating layer which is formed on the semiconductor substrate and on the circuit patterns (12s); and

a third insulating layer (14c) formed on the exposed first insulating layer (14a) and the second insulating layer. (See Fig. 5).

Thus, Yamaha is shown to teach all the features of the claim with the exception of explicitly show that the dummy area surrounding the circuit area.

However, Hosoda teaches that the dummy patterns (14a) can be formed any where on a chip including surrounding the circuit pattern at the edge of the chip.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the dummy patterns (13) of Yamaha surrounding the circuit patterns (12s) as taught by Hosoda to improve the planarity of the insulating layer near the edge of the chip.

Regarding the grid-line, it well known that at least one grid-line exists on any given chip formed on a semiconductor substrate to serve as a separation point for the chips.

*Product by process limitation*:

The expression "the width of the first (and third) dummy pattern is fixed by a concentration of solid content of the SOG (claims 3, 14 and 19); where a concentration of solid content of the SOG is around 5.2 wt% (claims 4, 10, 15 and 20); planarized by a thermal treatment (claim 5)" are taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Specifically, the "concentration of the solid content of the SOG" is clearly directed to process limitation. Likewise, the "planarizing by a thermal treatment" is also clearly directed to process limitation.

With respect to claim 2, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 3, the width of the first dummy pattern (13) of Yamaha appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 4, the width of the first dummy pattern (13) of Yamaha is designed for various size including less than 1μm. Additionally, since the SOG (14b) is formed in the spaces between the lines (12) of Yamaha, thus, it also encompass the claimed limitation.

With respect to claim 5, the device of Yamaha also includes multi-layered wiring; wherein the dummy pattern can be formed on the first and second level of a three levels wiring.

Thus, the semiconductor device of Yamaha is substantially similar as claimed including:

a second dummy pattern (13) formed under the first dummy pattern (13); and

a fourth insulating layer (14) formed directly on the substrate and on the second dummy pattern (13), the fourth insulating layer (14) having a planarized surface, whereby, the first dummy pattern is formed the fourth insulating layer which is formed on the second dummy pattern, and the circuit patterns (12) are formed on the fourth insulating layer.

With respect to claim 6, the shape and size of the second dummy pattern of Yamaha appears to be almost similar as those of the first dummy pattern, since the level is repeated.

With respect to claim 8, the second insulating layer (14b) of Yamaha is a SOG layer.

With respect to claim 9, the width of the first and second dummy patterns (13) of Yamaha appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 10, the width of the first and second dummy patterns (13) of Yamaha is designed for various size including less than 1μm. Additionally, since the SOG (14b) is formed in the spaces between the lines (12) of Yamaha, thus, it also encompass the claimed limitation.

With respect to claim 11, both Yamaha (Fig. 6) and Hosoda (Fig. 3) contemplate forming more than one dummy patterns on a same level, thus includes a third dummy pattern formed between the first dummy pattern and the circuit area. The embodiment of Fig. 5 of Yamaha is formed such that the insulating layer (14b) is not formed the first dummy pattern (13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the device of Yamaha having a third dummy pattern (13d) such that the insulating layer (14b) is not being formed on the first and third dummy pattern as well.

With respect to claim 12, the width of the third dummy pattern (13d) appears to be almost the same as that of the first dummy pattern.

With respect to claim 13, as best understood by the examiner, the dummy pattern (13) of Yamaha is formed in the region having spaces as claimed.

With respect to claim 14, the width of the first and third dummy patterns (13s) of Yamaha appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 15, the width of the first and third dummy patterns (13s) of Yamaha is designed for various size including less than 1μm. Additionally, since the SOG (14b) is formed in the spaces between the lines (12) of Yamaha, thus, it also encompass the claimed limitation.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha and Hosoda as applied to claim 5 above, and further in view of Hodate (JP-10-178011).

Yamaha and Hosoda teach all the features of the claim with the exception of forming the fourth insulating layer using BPSG material.

However, Hodate teaches that the fourth insulating layer (4) formed on the second dummy pattern (3) comprising BPSG.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to the fourth insulating layer covering the second dummy pattern of Yamaha using

BPSG as taught by Hodate to eliminate mobile ionic charge that might exist between the device layer and the metal layer.

8. Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaha and Hosoda as applied to claim 1 above, and further in view of Yang et al. (U.S. Patent No. 5,798,298).

With respect to claim 16, Yamaha and Hosoda teach all the features of the claim with the exception of a boding pad formed on the semiconductor substrate in the circuit area.

However, Yang teaches a semiconductor device including:

a bonding pad (30) formed on the semiconductor substrate (3) in the circuit area;

a fourth dummy pattern (34) surrounding the bonding pad. (See Fig. 3C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the semiconductor device of Yamaha having a bonding pad (30) as taught by Yang to making contact to the other devices.

With respect to "the first insulating layer being not formed on the fourth dummy pattern", the embodiment of Fig. 5 of Yamaha that the insulating layer (14b) is only formed over the circuit patterns not on the dummy pattern.

With respect to claim 17, the width of the fourth dummy pattern (34) of Yang appears to be almost the same as that of the first dummy pattern (34).

With respect to claim 18, the patterns of Yang is formed having spacing of 0.5 to 3 μm, thus, includes the claimed range.

With respect to claim 19, the width of the first and fourth dummy patterns (34s) of Yang appears to be fixed by a concentration of solid content of the SOG.

With respect to claim 20, the width of the first and fourth dummy patterns of Yamaha, in view of Yang, is designed for various size including less than 1μm. Additionally, since the SOG (14b) is formed in the spaces between the lines (12) of Yamaha, thus, it also encompass the claimed limitation.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
December 19, 2001

Douglas Wille
DOUGLAS WILLE